REMARKS

Amended Claims

Claims 63-65, 67 and 101 are amended herein.

Claim Rejections Under 35 U.S.C. § 102

Claim 83 was rejected under 35 U.S.C. § 102(a) as being anticipated by Applicants Admitted Prior Art (AAPA). Applicant respectfully traverses this rejection and submits that claim 83, as pending, is allowable for at least the following reasons.

The Office Action stated on Page 2, in rejecting claim 83 under 35 U.S.C. § 102(a), that "[a]pplicants admitted prior art discloses reading a physical page row [which includes user sectors and data sectors] from flash memory; transferring the selected data from the flash memory; masking off a first selected range of data column bit values and writing the selected range of data to a physical row of a target block (section 0043 of the specification)."

Applicant respectfully disagrees and maintains that paragraph [0043] of the Specification of the Present Application details a prior art "copy-back" command which does not transfer information from the flash memory device as recited in claim 83, but only reads information from the array to an internal data latch and then writes it back into the array to facilitate data fast transfers.

In particular, Applicant notes that paragraph [0043] states that "It is also noted that in a standard copy-back operation the data typically stays internal to the memory device and is not read out. Because of this, and the general overhead involved, the ECC codes are not evaluated. Thus, any memory device read errors or data corruption errors in the moved data, in either the user data of the moved sector or ECC data 314, will not be detected and/or corrected. Any such errors are generally copied into the target physical page verbatim, propagating the error forward and possibly contributing to deterioration of the data held in the memory device."

Applicant respectfully maintains that claim 83 recites, a method of moving data in a memory system comprising: reading one or more user data sectors and one or more overhead data areas of a physical page row of a source erase block from a selected non-volatile memory device of one or more non-volatile memory devices; transferring selected data of the one or more user data sectors and one or more overhead data areas from the selected non-volatile memory device; masking the one or more user data sectors and one or more overhead data areas; and

writing the one or more user data sectors and one or more overhead data areas to a physical page row of a target erase block."

Applicant respectfully contends that claim 83, as pending, has been shown to be patentably distinct from the Applicant's Admitted Prior Art (AAPA). Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(a) and allowance of claim 83.

Claim Rejections Under 35 U.S.C. § 103

Claims 63-64 and 68 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants Admitted Prior Art. Applicant respectfully traverses this rejection and submits that claims 63-64 and 68, as pending, are allowable for at least the following reasons.

In rejecting claims 63-64 and 68, the Office Action stated that "[a]pplicant's admitted prior art discloses reading a physical page row of a source block from a flash memory; transferring the selected data from the flash memory; masking off a first selected range of data column bit values and writing the selected range of data to a physical row of a target block (section 0043 of Applicant's specification). The admitted prior discloses a source block and a target block, however, the blocks are not a source erase block and a target erase block. The admitted prior art executes the above features when performing a data move operation wherein a subset of data read from a source block is written/moved to a target block, which provides efficiency since only the desired data is moved instead of the entire block. However, erase blocks are well known in the art in flash memory devices. Hence, it would have been obvious to one of ordinary skill in the art to perform the above features for erase blocks wherein only the desired data is erased instead of the entire source erase block, since only the selected masked data/overhead is moved to a target block, for the desirable purpose of efficiency."

Applicant respectfully disagrees and notes that Applicant's independent claim 63 is not directed towards moving erase blocks, but to moving selected data by reading a physical page row from a source erase block to internal data latches of a selected memory device, masking and then writing the data from the internal data latches to a physical page row of a target erase block of the selected memory device, while this occurs the selected data is also transferred from selected memory device. Applicant also respectfully disagrees with the Examiner's taking of official notice that moving erase blocks and moving physical pages or data blocks are similar

would be obvious to one skilled in the art and notes that physical pages are very different data structures from erase blocks.

In addition, as stated above, Applicant respectfully maintains that paragraph [0043] of the Specification of the Present Application details a prior art "copy-back" command which does not transfer information from the non-volatile memory device as recited in independent claim 63, but keeps the information internal to the non-volatile memory device, only transferring it from the array to an internal data latch and then back into the array. Applicant notes, in particular that paragraph [0043] specifically states that "It is also noted that in a standard copy-back operation the data typically stays internal to the memory device and is not read out. Because of this, and the general overhead involved, the ECC codes are not evaluated. Thus, any memory device read errors or data corruption errors in the moved data, in either the user data of the moved sector or ECC data 314, will not be detected and/or corrected. Any such errors are generally copied into the target physical page verbatim, propagating the error forward and possibly contributing to deterioration of the data held in the memory device."

As such, Applicant respectfully maintains that the AAPA does not teach or suggest all elements of claim 63, either alone or in combination with the examiner's taking of official notice.

Applicant respectfully contends that claim 63, as pending, has been shown to be patentably distinct from the cited references, either alone or in combination with the Examiner's taking of official notice. As claims 64 and 68 depend from and further define claim 63, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 63-64 and 68.

Claims 1-6, 29-32, 44, 67, 85-88 and 101 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Estakhri et al. (U.S. Patent No. 6,262,918 B1) in view of Applicants Admitted Prior Art (AAPA). Claims 7 and 33 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over Estakhri et al. (U.S. Patent No. 6,262,918 B1) in view of Applicants Admitted Prior Art and further in view of Danilak (U.S. Patent No. 7,117,421 B1). Applicant respectfully traverses these rejections and submits that claims 1-7, 29-33, 44, 67, 85-88 and 101, as pending, are allowable for at least the following reasons.

As stated above, Applicant respectfully maintains that paragraph [0043] of the Specification of the Present Application details a prior art "copy-back" command which does not

transfer information from the non-volatile memory device as recited in independent claim 63, but keeps the information internal to the non-volatile memory device, only transferring it from the array to an internal data latch and then back into the array. Applicant notes, in particular that paragraph [0043] specifically states that "It is also noted that in a standard copy-back operation the data typically stays internal to the memory device and is not read out."

In regards to Estakhri et al. – Applicant respectfully maintains that Estakhri et al. discloses only a parallel erasing Flash memory system that groups an erase block from each Flash memory device in the system into a larger group or "super block" to allow them to be erased in parallel, reducing the overall erase time from that of serially erasing the same number of erase blocks from a single Flash memory device. Applicant respectfully contends that Estakhri et al. does not disclose or suggest allocating erase blocks as part of super blocks or utilizing a super block grouping for storing information or split user/overhead data. *See, e.g.*, Estakhri et al., Figure 2; Column 2, Line 62 to Column 3, Line 54; and Column 9, Line 7 to Column 10, Line 23. Applicant further respectfully maintains that Estakhri et al.'s "super blocks" do not correspond to the definition of a super block in the Specification of the Present Application, which defines super blocks as pairs of erase blocks that store split data, where when user data is read from a sector of a first erase block of the Flash memory 200, the overhead data for the user data is read from the overhead data area of a sector of the second erase block of the erase block super block pair. *See*, Paragraphs [0010], [0025], [0035] and [0038] of the Specification of the Present Application.

As noted by the Examiner on Page 3 of the Non-Final Office Action mailed on May 1, 2007, Applicant respectfully maintains that Estakhri et al does not teach or suggest a non-split data move control circuit or a copy-back or a modified copy-back command.

As such, Applicant submits that combining the non-volatile memory device of Estakhri et al. with the copy-back command of the AAPA does not teach or suggest a non-volatile memory adapted to move one or more selected user data sectors and associated overhead data areas stored in one or more physical row pages of a selected source erase block to a target erase block in a modified copy-back move operation such that selected user data sectors and the associated overhead data areas stored in a source physical row page of the source erase block are moved to a target physical row page of the target erase block by reading the selected user data sectors and the associated overhead data areas into an internal latch of the at least one non-volatile memory device, transferring one or more latched user data sectors and associated overhead data areas from the at least one non-volatile memory device, masking the selected user data sectors and the

associated overhead data areas, and writing the selected user data sectors and the associated overhead data areas to the target physical row page.

Therefore Estakhri et al. and the AAPA do not teach or suggest each and every element of independent claims 1, 29, 44, 63, 85 and 101, either alone or in combination.

In regards to Danilak – Applicant respectfully maintains that Danilak discloses a memory controller that will automatically partition RAM memory devices into data and ECC areas and then read the data and ECC from a RAM memory device and correct the associated data transparently to the end user or processor. In this, Applicant respectfully maintains that Danilak only discloses evaluating the data and ECC codes as the data is accessed and read from the memory device and does not disclose or suggest evaluating the ECC as part of a data move operation where data is moved within a memory device from a source page to a target page or a source erase block to a target erase block. Applicant also respectfully maintains that Danilak does not disclose or suggest non-volatile memory devices or Flash memory devices that utilize an erase blocks. *See, e.g.*, Danilak, Figures 1, 4 and 5; Column 2, Line 44 to Column 3, Line 30; and Column 7, Line 9 to Column 8, Line 32.

As such, Applicant submits that combining the non-volatile memory device of Estakhri et al. with the copy-back command of the AAPA and the transparent ECC evaluation of Danilak also does not teach or suggest each and every element of independent claims 1 and 29 from which claims 7 and 33 depend, respectively, either alone or in combination, and therefore also do not teach or suggest claims 7 or 33.

Applicant respectfully contends that independent claims 1, 29, 44, 63, 85 and 101, as pending, have been shown to be patentably distinct from the cited references, either alone or in combination. As claims 2-7, 30-33, 67, 86-88 depend from and further define claims 1, 29, 63, and 85, respectively, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1-7, 29-33, 44, 67, 85-88 and 101.

Claims 63-64, 68 and 83 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwata et al. (U.S. Published Application No. 2004/0193774 A1) in view of Applicants Admitted Prior Art. Applicant respectfully traverses these rejections and submits that claims 163-64, 68 and 83, as pending, are allowable for at least the following reasons.

As stated above, Applicant respectfully maintains that paragraph [0043] of the Specification of the Present Application details a prior art "copy-back" command which does not

transfer information from the non-volatile memory device as recited in independent claim 63, but keeps the information internal to the non-volatile memory device, only transferring it from the array to an internal data latch and then back into the array. Applicant notes, in particular that paragraph [0043] specifically states that "It is also noted that in a standard copy-back operation the data typically stays internal to the memory device and is not read out."

In regards to Iwata et al. – Applicant respectfully maintains that Iwata et al. discloses a Flash memory card that has a Flash controller with an erase block data merge circuit which operates to consolidate data to a new erase block from an old erase block and subsequent erasure of the old erase block, which is accomplished by externally reading the data from the old erase block with the Flash controller and writing it to the new erase block. Applicant maintains that, in disclosing an external data merge circuit and operation, Iwata et al. does not disclose or suggest a non-split data move circuit or a Flash memory with an internal copy-back or an internal modified copy back command or operation or control circuits for managing the same. Applicant also maintains that Iwata et al. does not teach or suggest a data move operation that keeps the data internal to the non-volatile memory device for the move operation, yet also transfers it from the memory device and therefore also does not teach or suggest a data move operation for a non-volatile memory device that reads the data of a physical page row of a source erase block of the non-volatile memory device to internal data latches of the selected non-volatile memory device, transfers the selected data from the selected non-volatile memory device, masks off a first selected range of data column bit values in the internal data latches; and writes the first selected range of data column bit values from the internal data latches to a physical page row of a target erase block. As also noted by the Examiner, Iwata et al. also does not teach masking the read data. *See, e.g.*, Iwata et al., Abstract; Figures 1, 4 and 5; Paragraphs [0016]-[0079] and [0111]-[0142].

Applicant thus submits that Iwata et al. does not teach or suggest a split or a non-split data move circuit or method utilizing an internal modified copy back operation in a non-volatile memory. As such, Applicant submits that Iwata et al does not teach or suggest each and every element of the Applicant's claimed invention.

As such, Applicant submits that combining Flash memory card and controller of Iwata et al. with the copy-back command of the AAPA does not teach or suggest each and every element of independent claim 83 or 63, from which claims 64 and 68 depend, either alone or in combination.

Applicant respectfully contends that independent claims 63 and 83, as pending, have been shown to be patentably distinct from the cited references, either alone or in combination. As claims 64 and 68 depend from and further define claim 63, they are also considered to be in condition for allowance. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 63-64, 68 and 83.

Allowable Subject Matter

Applicant acknowledges that claims 8-28, 36-43, 45-62, 69-82, 84, 89-100 and 102 were indicated as being allowed in the Office Action.

Claims 34-35 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims.

Applicant respectfully submits that it has been shown in this Office Action response that independent base claim 29 has been shown to be patentably distinct from the cited references and is in condition for allowance. As such, claims 34-35 are also believed to be in condition for allowance in that these claims depend from and further define patentably distinct independent base claim 29. Applicant therefore respectfully requests reconsideration and withdrawal of the objections and allowance of claims 34-35.

CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. Please charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 501373.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

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